REMARKS/ARGUMENTS

Claims 46-120 remain pending. Previously examined claims 46, 48-51, 97, and 99-102 were rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-3 of USPN 6,429,481; claims 46-52, 54-58, 60-65, 67-73, 84, 86-87, 89, and 92-95, 97-103, 105-109, 111-113, and 118 were rejected under 35 USC 103(a) as being unpatentable over USPN 5,689,128 to Hshieh et al. (Hshieh '128) in view of USPN 6,165,826 to Chau et al. (Chau); and claims 53, 59, and 74-83, 85, 88, 90-91, 96, 96, 104, 110, and 119-120 were rejected under 35 USC 103(a) as being unpatentable over Hshieh '128 in view of Chau and USPN 6,204,533 to Williams et al. (Williams '533). Applicants respectfully traverse these rejections and request reconsideration of the claims.

Double Patenting

Applicants herewith submit a terminal disclaimer under 37 CFR 1.321(c) obviating the obviousness-type double patenting rejection over USPN 6,429,481. Accordingly, withdrawal of this rejection is respectfully requested.

Claim Rejections - 35 USC § 103

- Hshieh '128 in view of Chau

Claims 46-52, 54-58, 60-65, 67-73, 84, 86-87, 89, and 92-95, 97-103, 105-109, 111-113, and 118 stand rejected under 35 USC 103(a) as being unpatentable over Hshieh '128 in view of Chau. With respect to independent claims 46, 67, and 97, the rejection states that Hshieh '128 discloses all of the claimed elements in Figure 3 but fails to expressly describe an abrupt junction for the heavily doped region. The rejection then adds "But the structure of the deeper doped well and a second well of an opposite dopant may create an abrupt junction as claimed. For example, Chau, in fig. 2, discloses a transistor, CMOS, and the structure includes shallow doped regions of the opposite dopants. This set up with the ultra shallow tip can be characterized as an abrupt junction in order to facilitate hot carrier injection." Applicants respectfully traverse this rejection.

- Combining Hshieh '128 and Chau does not result in claimed structure

The rejection states that Hshieh '128 "does not expressly describe the junction as being an abrupt junction." Applicants are in agreement with this statement. However, the rejection further states that "It should be noted that even though the cited reference does not mention the function of the heavily doped region as abrupt junction. But the structure of the deeper doped well and a second well *of an opposite dopant* may create an abrupt junction as claimed." (emphasis added) This statement is flawed for a number of reasons.

First, to reiterate, there is no junction in any of the embodiments in Hshieh '128 that is defined either expressly, inherently, impliedly or in any other fashion as being abrupt. While an opposite polarity junction *may* create an abrupt junction, absent an affirmative teaching of an abrupt junction, one of ordinary skill in the art would commonly assume a linearly graded junction since an abrupt junction requires special processing. Applicants have previously submitted explanations in support of this point at length and will not repeat them here.

The above statement by the rejection, however, on its face contradicts the rest of the rejection's analysis. The junction that is characterized as being abrupt by the claims is the junction formed between "a doped well having dopants of a second conductivity type" and "a doped heavy body region having dopants of the second conductivity type." (Claim 46) The claimed abrupt junction is therefore between two regions having dopants of *the same* not opposite conductivity type. The rejection also starts out by alleging regions 14 and 18 in figure 3 of Hshieh '128, which have the same conductivity type, as corresponding to the claimed regions. Thus, the statement "But the structure of the deeper doped well and a second well *of an opposite dopant* may create an abrupt junction as claimed" is not only not applicable to the claimed structure, it is in direct contradiction to the rest of the analysis by the rejection.

This contradiction in the rejection's rationale may have been caused by the fact that the abrupt junction in the secondary reference, Chau, is between two opposite polarity regions. Chau's abrupt junction is between the source/drain region 210 and the substrate or well

201, i.e., between two opposite polarity regions. Chau, col. 4, line 47, to col. 5, line 2. Combining Chau with Hshieh '128 would therefore result in making the opposite polarity junction between source region 20 (n+) and well region 14 (p) in Hshieh '128 to be abrupt, and not the same polarity junction between body contact region 18 (p+) and well 14 (p). Thus, combining Hshieh '128 with Chau to reject the claims of the present invention is improper for this as well as other reasons explained below.

- No Suggestion or Motivation to Combine

To establish a *prima facie* case of obviousness it is essential to find some motivation or suggestion to make the claimed invention in light of the prior art teachings. *In re Brouwer, 77 F.3d 422, 425 (Fed. Cir. 1996).* The rejection states that "Chau, in fig. 2, discloses a transistor, CMOS, and the structure includes shallow doped regions of the opposite dopants. This set up with the ultra shallow tip can be characterized as an abrupt junction in order to facilitate hot carrier injection. ... Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made [sic] to recognize the structure that could create such junction as taught by Chau in Hshieh's device in order to take the advantage as mentioned." Applicants respectfully disagree with this analysis and submit that it is erroneous in a number of respects.

First, the purported motivation to combine as stated by the rejection is Chau's use of "an abrupt junction in order to facilitate hot carrier injection." However, to the extent Chau may discuss hot electron effects at all, such discussion is in no way related to any abrupt junction. The only two references to hot electron effects that could be found in Chau are reproduced below:

> Silicon nitride layer 314 is preferably formed by a "hot-wall" process to provide a very hermetic seal of gate electrodes 306 and 308, and the edges of gate dielectric 303. By forming silicon nitride layer 314 directly onto gate electrode 306 and 308, a hermetic seal is formed and the hot electron lifetime of the fabricate transistors dramatically improved. Chau, col. 7, lines 21-27.

> Hot-wall silicon nitride layer is preferred in order to provide a hermetic seal of gate electrodes 306 and 308 and the edges of gate oxide layer 303 to thereby reduce hot electron effects of the fabricated transistor. Chau, col. 13, lines 6-9.

Thus, Chau teaches a process for hermetically sealing the gate electrode of a transistor to "reduce" hot electron effects of the transistor. Chau therefore teaches not only the opposite of "facilitating" hot electron injection, it's discussion of hot electron effects is not in any way related to any abrupt junctions in the transistor. The purported motivation to combine Chau's abrupt junction with Hshieh '128 - to facilitate hot carrier injection -, as stated by the rejection, is therefore not only inapplicable but clearly erroneous.

- Chau Teaches Away from the Invention

Chau does disclose the use of an abrupt junction, but it does so in a fundamentally different device structure and for very different purposes. Chau is primarily concerned with the manufacture of very short channel transistors in order to increase transistor density for ultra large-scale integrated CMOS circuits, without increasing parasitic resistance or compromising punch-though characteristics of the transistors. [Chau, col. 1, lines 24-32, and 47-60]. To accomplish this, Chau proposes forming a source/drain extension 210 with an ultra shallow tip portion 214 and a raised tip portion 216 in transistor 200 shown in Figure 2. Chau provides:

> It is to be appreciated that because novel methods of fabrication are employed in the present invention, ultra shallow tip 214 can be characterized by a very abrupt junction. Col. 4, line 66, to col. 5, line 2.

> It is to be appreciated that a valuable feature of the present invention is the fact that transistor 200 includes a tip or source/drain extension 210 which is both ultra shallow and raised. In this way, transistor 200 has a shallow tip with a very low parasitic resistance. The novel structure of transistor 200 allows for tip scaling necessary for the fabrication of transistor 200 with effective gate length less than 0.12 μm. Because of the novel tip structure 210 of the present invention, transistor 200 has good punchthrough performance and reduced V_T roll-off. Additionally, because of tip 210, transistor 200 has a low parasitic resistance, resulting in good drive current. Col. 5, lines 35-45.

Thus, according to Chau, the abrupt junction helps enable fabrication of transistors with shorter channel (or smaller gate length) with good punch-through performance and low parasitic resistance.

A number of significant differences between Chau's transistor and the claimed transistor should become apparent from the above. As already noted above, Chau's abrupt junction is between the source/drain region 210 and the substrate or well 201, i.e., between two opposite polarity regions. Chau, col. 4, line 47, to col. 5, line 2. Combining Chau with Hshieh '128 would therefore result in making the opposite polarity junction between source region 20 (n+) and well region 14 (p) in Hshieh '128 to be abrupt, and not the same polarity junction between body contact region 18 (p+) and well 14 (p). In contrast, the present invention as set forth in, for example, claim 46, recites a transistor "wherein the heavy body region forms an abrupt junction in the doped well."

Further, Chau's transistor is intended for "ultra large-scale integration" of CMOS circuits and not discrete trench gated power devices. A very different set of performance characteristics are required from a trench gated power transistor as compared to a planar transistor in a CMOS integrated circuit. For example, in a trench gated device such as claimed by the present invention, a concern to be addressed is damage to gate oxide due to concentration of electric fields at corners of the trenches inside the body of the silicon. One benefit of the presently claimed abrupt junction formed between the heavy body region and the well is that it attracts and therefore moves the peak electric filed away from the trench corners. The abrupt junction of the present invention thus lowers the breakdown voltage at the location of the abrupt junction.

One of Chau's primary goals is to improve (i.e., increase) transistor breakdown voltage. Improvement in punch-through performance of Chau's transistor is purportedly achieved by increasing the spacing between the source/drain regions on either sides of the channel, i.e., the formation of an abrupt junction at the source/drain to channel region reduces

out-diffusion affects that would otherwise make the channel shorter than intended. This is consistent with the fact that according to Chau it is the PMOS transistor (which has source/drains formed by highly diffusive Boron atoms) that is fabricated with the ultra shallow tip and not the NMOS transistor (which has source/drains formed by slow diffusing Arsenic atoms) which is fabricated as a "conventional NMOS transistor." Chau, col. 5, lines 51-54. Thus, whereas the abrupt junction of the present invention lowers breakdown voltage at the location of the abrupt junction, Chau's abrupt junction in the ultra shallow trip allows for larger source/drain spacing which is intended to increase (not lower) the transistor breakdown voltage of the transistor.

Chau's abrupt junction thus differs from the claimed abrupt junction not only because it is formed between source/drain and well/substrate regions that are of opposite polarity, but because it is intended to increase breakdown voltage by increasing source/drain spacing, as opposed to decrease breakdown voltage at the location of the abrupt junction. The combination of Chau and Hshieh '128 thus teaches away from the present invention as claimed.

- Chau is Nonanalogous Art

By now it should be apparent that Chau which focuses on transistor technology for ultra large-scale integrated CMOS circuits with both PMOS and NMOS transistors having planar gate structures is nonanalogous to trench gated discrete devices of the type described by Hshieh '128 or the present invention. Chau's transistors are thus intended for an entirely different type of application than those of Hshieh '128 or the present invention. Merely because Chau discusses transistors it does not make it necessarily in the same field of endeavor as Hshieh '128 or the present invention. *Medtronic, Inc. v. Cardiac Pacemakers, 721 F.2d 1563 (Fed. Cir. 1983); Wang Laboratories, Inc. v. Toshiba Corp. 993 F.2d 858 (Fed. Cir. 1993).* One of ordinary skill in this art would therefore not combine the teachings of Chau with Hshieh '128.

Accordingly, combining Chua and Hshieh '128 to reject independent claims 46, 67 and 97 is improper not only because the combination does not result in the claimed structure, but also because there is no motivation or suggestion to combine the two references, and because

Chau teaches away from the combination, and because Chau is nonanalogous art. Independent claims 46, 67 and 97 are patentable over the cited references for at least these reasons. While the rejected dependent claims recite additional novel and non-obvious features that further distinguish over the cited references, they ultimately depend from one of the three independent claims 46, 67 and 97 and thus derive patentability at least from the combination recited in those claims. Withdrawal of this rejection is respectfully requested.

- Hshieh '128 and Chau further in view of Williams '533

Claims 53, 59, and 74-83, 85, 88, 90-91, 96, 96, 104, 110, and 119-120 stand rejected under 35 USC 103(a) as being unpatentable over Hshieh '128 and Chau further in view of Williams '533. Applicants respectfully traverse this rejection as with all other claims above. As explained above, all three independent claims 46, 67 and 97 are patentable over the two primary references Hshieh '128 and Chau. Williams '533 does not cure the deficiencies of Hshieh '128 and Chau. While the rejected dependent claims recite additional novel and non-obvious features that further distinguish over the cited references, they ultimately depend from one of the three independent claims 46, 67 and 97 and thus derive patentability at least from the combination recited in those claims. Withdrawal of this rejection is respectfully requested.

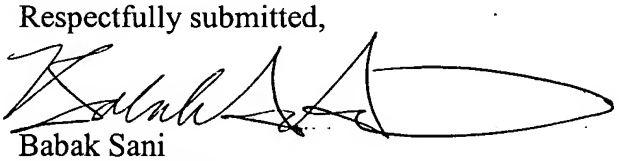
CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

Authorization is given to charge any fees that may be required to the undersigned's Deposit Account No. 20-1430.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,



Babak Sani
Reg. No. 45,068

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: 415-576-0200
Fax: 415-576-0300
BSS:deb
Attachments
60917506 v1